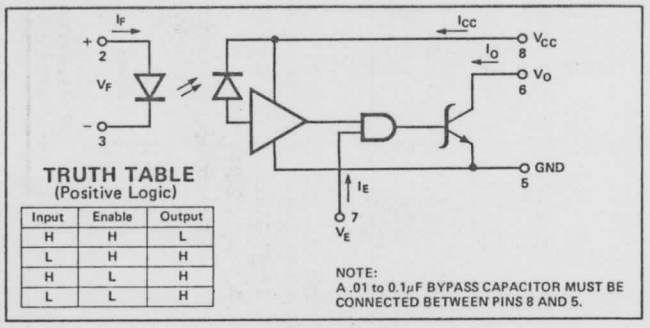
HEWLETT hp PACKARD

COMPONENTS

# LSTTL/TTL COMPATIBLE OPTOCOUPLER

# 6N137

TECHNICAL DATA APRIL 1979




**TRUTH TABLE**
(Positive Logic)

| Input | Enable | Output |
|---|---|---|
| H | H | L |
| L | H | H |
| H | L | H |
| L | L | H |

NOTE:
A .01 to 0.1μF BYPASS CAPACITOR MUST BE CONNECTED BETWEEN PINS 8 AND 5.

**Figure 1.**

## Features

- **LSTTL/TTL COMPATIBLE: 5V SUPPLY**
- **ULTRA HIGH SPEED**
- **LOW INPUT CURRENT REQUIRED**
- **HIGH COMMON MODE REJECTION**
- **GUARANTEED PERFORMANCE OVER TEMPERATURE**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361)**
- **3000V dc INSULATION VOLTAGE**

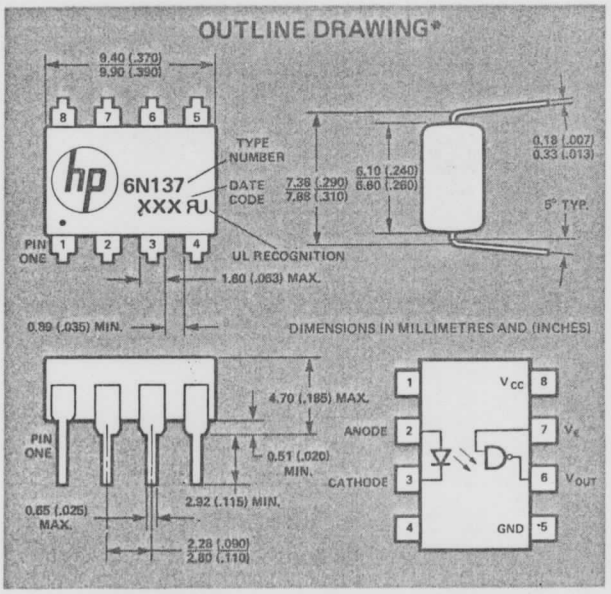
## Description Applications

The 6N137 consists of a GaAsP photon emitting diode and a unique integrated detector. The photons are collected in the detector by a photodiode and then amplified by a high gain linear amplifier that drives a Schottky clamped open collector output transistor. The circuit is temperature, current and voltage compensated.

This unique isolator design provides maximum DC and AC circuit isolation between input and output while achieving LSTTL/TTL circuit compatibility. The isolator operational parameters are guaranteed from 0°C to 70°C, such that a minimum input current of 5mA will sink an eight gate fan-out (13mA) at the output with 5 volt $V_{CC}$ applied to the detector. This isolation and coupling is achieved with a typical propagation delay of 45ns. The enable input provides gating of the detector with input sinking and sourcing requirements compatible with LSTTL/TTL interfacing and a propagation delay of 25ns typical.

The 6N137 can be used in high speed digital interfacing applications where common mode signals must be rejected, such as for a line receiver and digital programming of floating power supplies, motors, and other machine control systems. The elimination of ground loops can be accomplished in system interfaces such as between a computer and a peripheral memory, printer, controller, etc.

The open collector output provides capability for bussing, OR'ing and strobing.




## Recommended Operating Conditions

| | Sym. | Min. | Max. | Units |
|---|---|---|---|---|
| Input Current, Low Level Each Channel | $I_{FL}$ | 0 | 250 | μA |
| Input Current, High Level Each Channel | $I_{FH}$ | 6.3** | 15 | mA |
| High Level Enable Voltage | $V_{EH}$ | 2.0 | $V_{CC}$ | V |
| Low Level Enable Voltage (Output High) | $V_{EL}$ | 0 | 0.8 | V |
| Supply Voltage, Output | $V_{CC}$ | 4.5 | 5.5 | V |
| Fan Out (TTL Load) | N | | 8 | |
| Operating Temperature | $T_A$ | 0 | 70 | °C |

## Absolute Maximum Ratings*

(No derating required up to 70°C)

Storage Temperature ..... −55°C to +125°C
Operating Temperature ..... 0°C to +70°C
Lead Solder Temperature ..... 260°C for 10s
(1.6mm below seating plane)
Peak Forward Input Current ..... 40mA (1≤ 1msec Duration)
Average Forward Input Current ..... 20mA
Reverse Input Voltage ..... 5V
Enable Input Voltage ..... 5.5V
(Not to exceed $V_{CC}$ by more than 500mV)
Supply Voltage - $V_{CC}$ ..... 7V (1 Minute Maximum)
Output Current - $I_O$ ..... 50mA
Output Collector Power Dissipation ..... 85mW
Output Voltage - $V_O$ ..... 7V

**6.3mA condition permits at least 20% CTR degradation guardband. Initial switching threshold is 5mA or less.

*JEDEC Registered Data.

# Electrical Characteristics

## OVER RECOMMENDED TEMPERATURE ($T_A$ = 0°C TO 70°C) UNLESS OTHERWISE NOTED

| Parameter | Symbol | Min. | Typ.** | Max. | Units | Test Conditions | Figure | Note |
|---|---|---|---|---|---|---|---|---|
| High Level Output Current | $I_{OH}$* | | 50 | 250 | μA | $V_{CC}$=5.5V, $V_O$=5.5V, $I_F$=250μA, $V_E$=2.0V | 6 | |
| Low Level Output Voltage | $V_{OL}$* | | 0.5 | 0.6 | V | $V_{CC}$=5.5V, $I_F$=5mA, $V_{EH}$=2.0V $I_{OL}$ (Sinking) =13mA | 3,5 | |
| High Level Enable Current | $I_{EH}$ | | -1.0 | | mA | $V_{CC}$=5.5V, $V_E$=2.0V | | |
| Low Level Enable Current | $I_{EL}$* | | -1.6 | -2.0 | mA | $V_{CC}$=5.5V, $V_E$=0.5V | | |
| High Level Supply Current | $I_{CCH}$* | | 7 | 15 | mA | $V_{CC}$=5.5V, $I_F$=0 $V_E$=0.5V | | |
| Low Level Supply | $I_{CCL}$* | | 13 | 18 | mA | $V_{CC}$=5.5V, $I_F$=10mA $V_E$=0.5V | | |
| Input-Output Insulation Leakage Current | $I_{I-O}$* | | | 1.0 | μA | Relative Humidity=45% $T_A$=25°C, t=5s $V_{I-O}$=3000Vdc | | 5 |
| Resistance (Input-Output) | $R_{I-O}$ | | $10^{12}$ | | Ω | $V_{I-O}$=500V, $T_A$=25°C | | 5 |
| Capacitance (Input-Output) | $C_{I-O}$ | | 0.6 | | pF | f=1MHz, $T_A$=25°C | | 5 |
| Input Forward Voltage | $V_F$* | | 1.5 | 1.75 | V | $I_F$=10mA, $T_A$=25°C | 4 | 8 |
| Input Reverse Breakdown Voltage | $BV_R$* | 5 | | | V | $I_R$=10μA, $T_A$=25°C | | |
| Input Capacitance | $C_{IN}$ | | 60 | | pF | $V_F$=0, f=1MHz | | |
| Current Transfer Ratio | CTR | | 700 | | % | $I_F$=5.0mA, $R_L$=100Ω | 2 | 7 |

**All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C



# Switching Characteristics at $T_A$=25°C, $V_{CC}$=5V

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions | Figure | Note |
|---|---|---|---|---|---|---|---|---|
| Propagation Delay Time to High Output Level | $t_{PLH}$* | | 45 | 75 | ns | $R_L$=350Ω, $C_L$=15pF, $I_F$=7.5mA | 7,9 | 1 |
| Propagation Delay Time to Low Output Level | $t_{PHL}$* | | 45 | 75 | ns | $R_L$=350Ω, $C_L$=15pF, $I_F$=7.5mA | 7,9 | 2 |
| Output Rise-Fall Time (10-90%) | $t_r$, $t_f$ | | 25 | | ns | $R_L$=350Ω, $C_L$=15pF, $I_F$=7.5mA | | |
| Propagation Delay Time of Enable from $V_{EH}$ to $V_{EL}$ | $t_{ELH}$ | | 25 | | ns | $R_L$=350Ω, $C_L$=15pF, $I_F$=7.5mA, $V_{EH}$=3.0V, $V_{EL}$=0.5V | 8 | 3 |
| Propagation Delay Time of Enable from $V_{EL}$ to $V_{EH}$ | $t_{EHL}$ | | 15 | | ns | $R_L$=350Ω, $C_L$=15pF, $I_F$=7.5mA $V_{EH}$=3.0V, $V_{EL}$=0.5V | 8 | 4 |
| Common Mode Transient Immunity at Logic High Output Level | $CM_H$ | | 50 | | v/μs | $V_{CM}$=10V $R_L$=350Ω, $V_O$ (min.)=2V, $I_F$=0mA | 11 | 6 |
| Common Mode Transient Immunity at Logic Low Output Level | $CM_L$ | | -150 | | v/μs | $V_{CM}$=10V $R_L$=350Ω, $V_O$ (max.)=0.8V, $I_F$=5mA | 11 | 6 |

*JEDEC Registered Data.

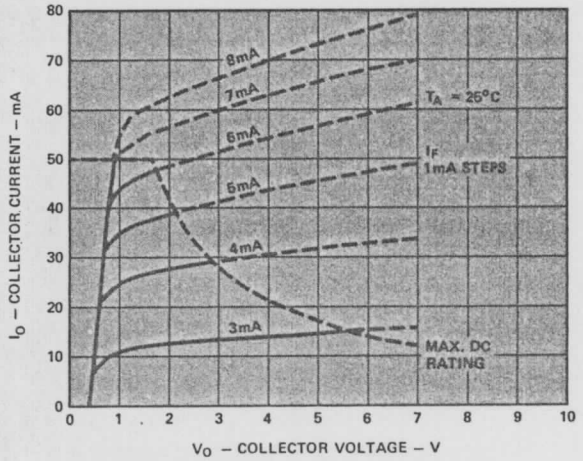
# Operating Procedures and Definitions

**Logic Convention.** The 6N137 is defined in terms of positive logic.

**Bypassing.** A ceramic capacitor (.01 to 0.1μF) should be connected from pin 8 to pin 5 (Figure 12). Its purpose is to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching properties. The total lead length between capacitor and coupler should not exceed 20mm.

**Polarities.** All voltages are referenced to network ground (pin 5). Current flowing toward a terminal is considered positive.

**Enable Input.** No external pull-up required for a logic (1), i.e., can be open circuit.




Note: Dashed characteristics — denote pulsed operation only.

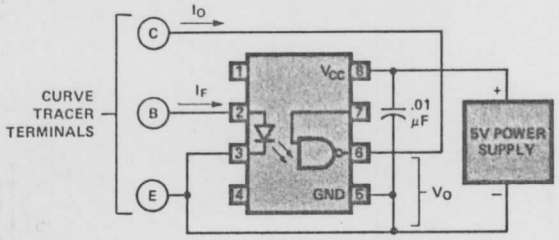
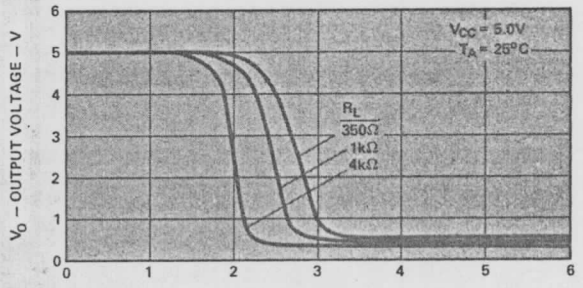



**Figure 2. Optocoupler Collector Characteristics.**



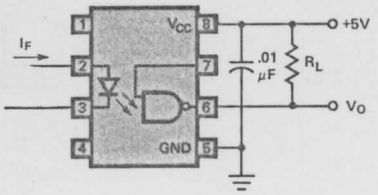




**Figure 3. Input-Output Characteristics.**

**NOTES:**

1. The $t_{PLH}$ propagation delay is measured from the 3.75mA point on the trailing edge of the input pulse to the 1.5V point on the trailing edge of the output pulse.
2. The $t_{PHL}$ propagation delay is measured from the 3.75mA point on the leading edge of the input pulse to 1.5V point on the leading edge of the output pulse.
3. The $t_{ELH}$ enable propagation delay is measured from the 1.5V point of the trailing edge of the input pulse to the 1.5V point on the trailing edge of the output pulse.
4. The $t_{EHL}$ enable propagation delay is measured from the 1.5V point on the leading edge of the input pulse to the 1.5V point on the leading edge of the output pulse.
5. Device considered a two terminal device: pins 2 and 3 shorted together, and pins 5, 6, 7, and 8 shorted together.
6. Common mode transient immunity in Logic High level is the maximum tolerable (positive) $dV_{CM}/dt$ on the leading edge of the common mode pulse, $V_{CM}$, to assure that the output will remain in a Logic High state (i.e., $V_O > 2.0V$). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) $dV_{CM}/dt$ on the trailing edge of the common mode pulse signal, $V_{CM}$, to assure that the output will remain in a Logic Low state (i.e., $V_O < 0.8V$).
7. DC Current Transfer Ratio is defined as the ratio of the output collector current to the forward bias input current times 100%.
8. At 10mA $V_F$ decreases with increasing temperature at the rate of 1.6mV/°C.

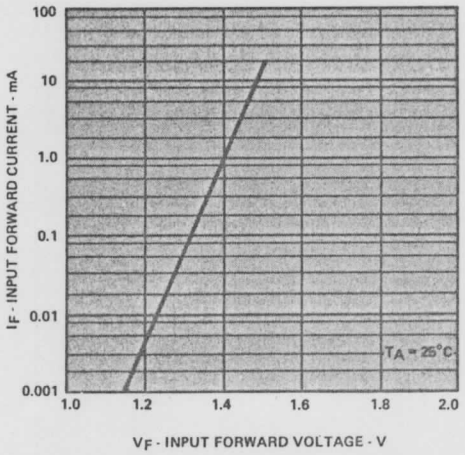



**Figure 4. Input Diode Forward Characteristic.**

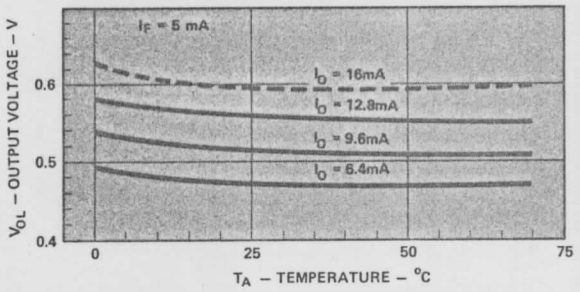



**Figure 5. Output Voltage, $V_{OL}$ vs. Temperature and Fan-Out.**

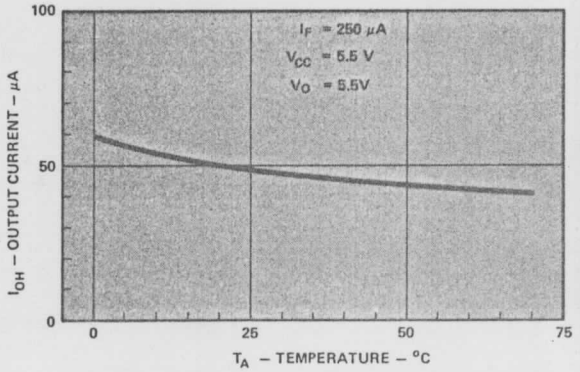



**Figure 6. Output Current, $I_{OH}$ vs. Temperature ($I_F$=250μA).**

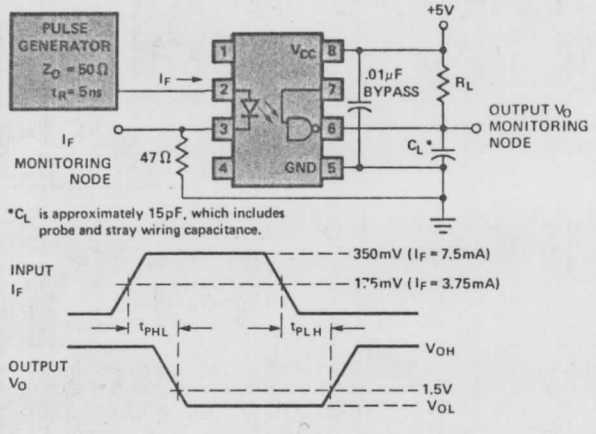



Figure 7. Test Circuit for $t_{PHL}$ and $t_{PLH}$.**

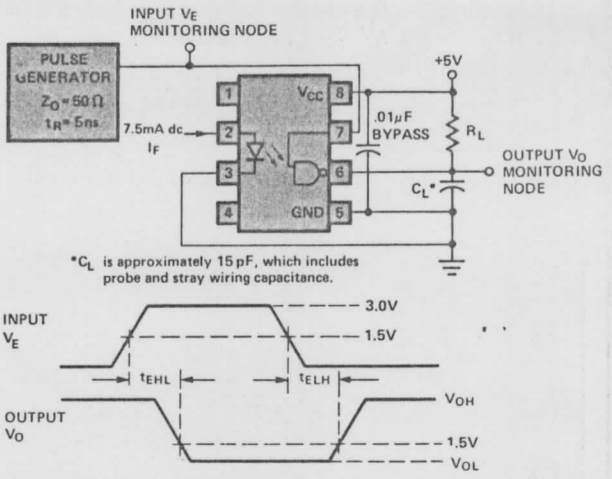



Figure 8. Test Circuit for $t_{ELH}$ and $t_{EHL}$.

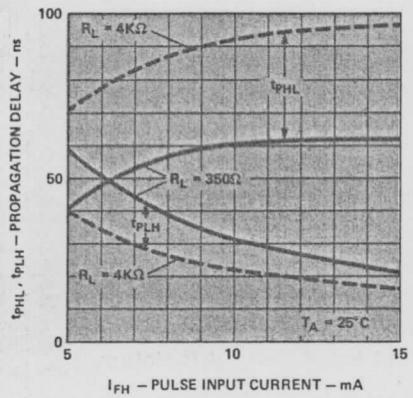



Figure 9. Propagation Delay, $t_{PHL}$ and $t_{PLH}$ vs. Pulse Input Current, $I_{FH}$.

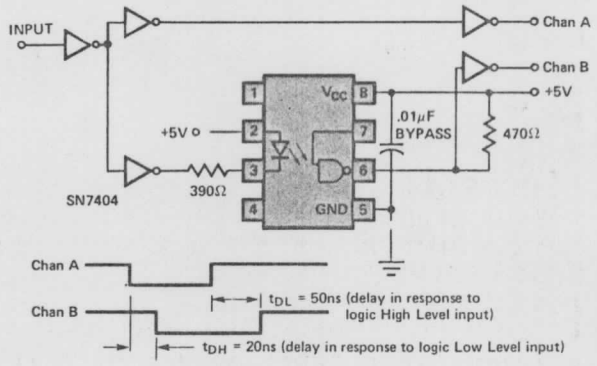
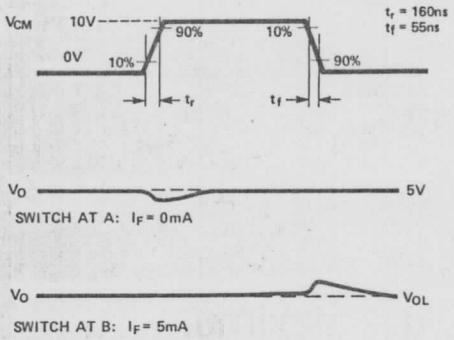



Figure 10. Response Delay Between TTL Gates.



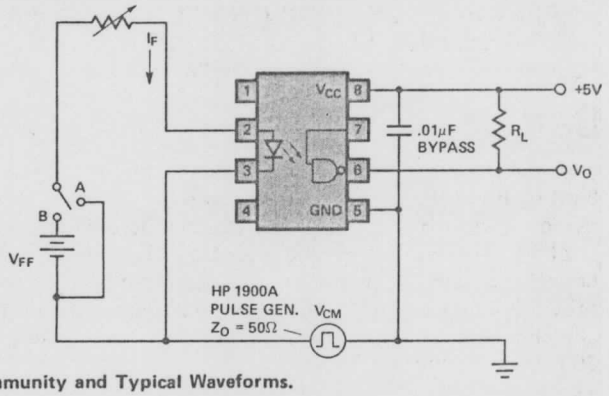




Figure 11. Test Circuit for Transient Immunity and Typical Waveforms.

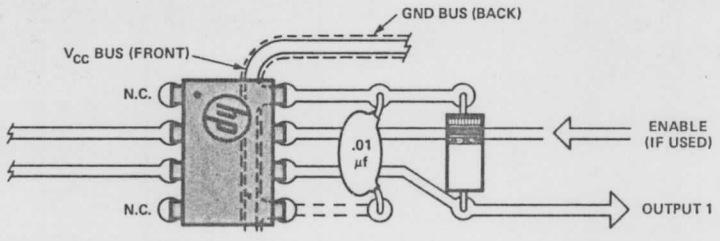



Figure 12. Recommended Printed Circuit Board Layout.

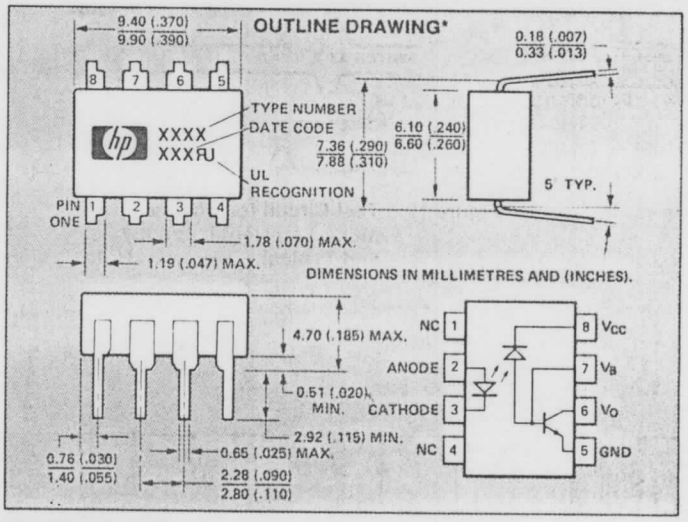
** JEDEC Registered Data.

HEWLETT PACKARD

# LOW INPUT CURRENT, HIGH GAIN OPTOCOUPLERS

6N138
6N139

TECHNICAL DATA JANUARY 1984




## Features

- HIGH CURRENT TRANSFER RATIO — 800% TYPICAL
- LOW INPUT CURRENT REQUIREMENT — 0.5 mA
- TTL COMPATIBLE OUTPUT — 0.1 V $V_{OL}$ TYPICAL
- HIGH COMMON MODE REJECTION — 500 V/$\mu$s
- PERFORMANCE GUARANTEED OVER TEMPERATURE 0° C to 70° C
- BASE ACCESS ALLOWS GAIN BANDWIDTH ADJUSTMENT
- HIGH OUTPUT CURRENT — 60 mA
- 100K BITS/SEC TYPICAL SPEED AT $I_F$ = 0.5 mA
- DIELECTRIC WITHSTAND TESTED AT 3000 Vdc FOR A WORKING VOLTAGE OF 220 Vac
- RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361)

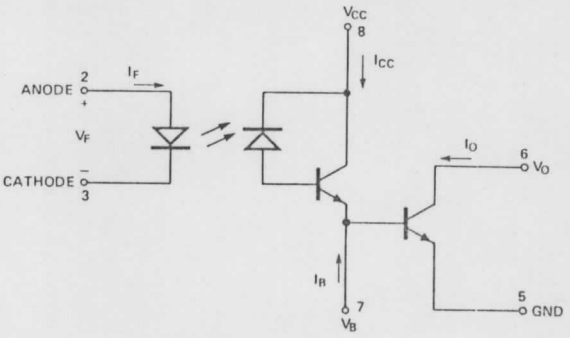
## Description

These high gain series couplers use a Light Emitting Diode and an integrated high gain photon detector to provide extremely high current transfer ratio between input and output. Separate pins for the photodiode and output stage result in TTL compatible saturation voltages and high speed operation. Where desired the Vcc and Vo terminals may be tied together to achieve conventional photodarlington operation. A base access terminal allows a gain bandwidth adjustment to be made.

The 6N139 is suitable for use in CMOS, LSTTL or other low power applications. A 400% minimum current transfer ratio is guaranteed over a 0-70° C operating range for only 0.5 mA of LED current.

The 6N138 is suitable for use mainly in TTL applications. Current Transfer Ratio is 300% minimum over 0-70° C for an LED current of 1.6 mA [1 TTL unit load (U.L.)]. A 300% minimum CTR enables operation with 1 U.L. in, 1 U.L. out with a 2.2 kΩ pull-up resistor.

SCHEMATIC




## Applications

- Ground Isolate Most Logic Families — TTL/TTL, CMOS/TTL, CMOS/CMOS, LSTTL/TTL, CMOS/LSTTL
- Low Input Current Line Receiver — Long Line or Party line
- EIA RS-232C Line Receiver
- Telephone Ring Detector
- 117 V ac Line Voltage Status Indicator — Low Input Power Dissipation
- Low Power Systems — Ground Isolation

## Absolute Maximum Ratings*

Storage Temperature . . . . . −55°C to +125°C
Operating Temperature . . . . . 0°C to +70°C
Lead Solder Temperature . . . . . 260°C for 10s
(1.6mm below seating plane)
Average Input Current — $I_F$ . . . . . 20mA [1]
Peak Input Current — $I_F$ . . . . . 40mA
(50% duty cycle, 1 ms pulse width)
Peak Transient Input Current — $I_F$ . . . . . 1.0A
(≤ 1$\mu$s pulse width, 300 pps)
Reverse Input Voltage — $V_R$ . . . . . 5V
Input Power Dissipation . . . . . 35mW [2]
Output Current — $I_O$ (Pin 6) . . . . . 60mA [3]
Emitter-Base Reverse Voltage (Pin 5-7) . . . . . 0.5V
Supply and Output Voltage — $V_{CC}$ (Pin 8-5), $V_O$ (Pin 6-5)
6N138 . . . . . −0.5 to 7V
6N139 . . . . . −0.5 to 18V
Output Power Dissipation . . . . . 100mW [4]

See notes, following page.

*CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

*JEDEC Registered Data.

# Electrical Specifications

## OVER RECOMMENDED TEMPERATURE ($T_A$ = 0°C to 70°C), UNLESS OTHERWISE SPECIFIED

| Parameter | Sym. | Device | Min. | Typ.** | Max. | Units | Test Conditions | Fig. | Note |
|---|---|---|---|---|---|---|---|---|---|
| Current Transfer Ratio | CTR* | 6N139 | 400<br>500 | 800<br>900 | | % | $I_F$ = 0.5mA, $V_O$ = 0.4V, $V_{CC}$ = 4.5V<br>$I_F$ = 1.6mA, $V_O$ = 0.4V, $V_{CC}$ = 4.5V | 3 | 5,6 |
| | | 6N138 | 300 | 600 | | % | $I_F$ = 1.6mA, $V_O$ = 0.4V, $V_{CC}$ = 4.5V | | |
| Logic Low Output Voltage | $V_{OL}$ | 6N139 | | 0.1<br>0.1<br>0.2 | 0.4<br>0.4<br>0.4 | V | $I_F$ = 1.6mA, $I_O$ = 6.4mA, $V_{CC}$ = 4.5V<br>$I_F$ = 5mA, $I_O$ = 15mA, $V_{CC}$ = 4.5V<br>$I_F$ = 12mA, $I_O$ = 24mA, $V_{CC}$ = 4.5V | 1,2 | 6 |
| | | 6N138 | | 0.1 | 0.4 | V | $I_F$ = 1.6mA, $I_O$ = 4.8mA, $V_{CC}$ = 4.5V | | |
| Logic High Output Current | $I_{OH}$* | 6N139 | | 0.05 | 100 | μA | $I_F$ = 0mA, $V_O$ = $V_{CC}$ = 18V | | 6 |
| | | 6N138 | | 0.1 | 250 | μA | $I_F$ = 0mA, $V_O$ = $V_{CC}$ = 7V | | |
| Logic Low Supply Current | $I_{CCL}$ | | | 0.2 | | mA | $I_F$ = 1.6mA, $V_O$ = Open, $V_{CC}$ = 5V | | 6 |
| Logic High Supply Current | $I_{CCH}$ | | | 10 | | nA | $I_F$ = 0mA, $V_O$ = Open, $V_{CC}$ = 5V | | 6 |
| Input Forward Voltage | $V_F$* | | | 1.4 | 1.7 | V | $I_F$ = 1.6mA, $T_A$ = 25°C | 4 | |
| Input Reverse Breakdown Voltage | $BV_R$* | | 5 | | V | | $I_R$ = 10μA, $T_A$ = 25°C | | |
| Temperature Coefficient of Forward Voltage | $\frac{\Delta V_F}{\Delta T_A}$ | | | −1.8 | | mV/°C | $I_F$ = 1.6mA | | |
| Input Capacitance | $C_{IN}$ | | | 60 | | pF | f = 1MHz, $V_F$ = 0 | | |
| Input - Output Insulation Leakage Current | $I_{I-O}$* | | | | 1.0 | μA | 45% Relative Humidity, $T_A$ = 25°C<br>t = 5 s, $V_{I-O}$ = 3000Vdc | | 7,11 |
| Resistance (Input-Output) | $R_{I-O}$ | | | $10^{12}$ | | Ω | $V_{I-O}$ = 500Vdc | | 7 |
| Capacitance (Input-Output) | $C_{I-O}$ | | | 0.6 | | pF | f = 1MHz | | 7 |

**All typicals at $T_A$ = 25°C and $V_{CC}$ = 5V, unless otherwise noted.

# Switching Specifications

## AT $T_A$ = 25°C

| Parameter | Sym. | Device | Min. | Typ. | Max. | Units | Test Conditions | Fig. | Note |
|---|---|---|---|---|---|---|---|---|---|
| Propagation Delay Time To Logic Low at Output | $t_{PHL}$* | 6N139 | | 5<br>0.2 | 25<br>1 | μs | $I_F$ = 0.5mA, $R_L$ = 4.7kΩ<br>$I_F$ = 12mA, $R_L$ = 270Ω | 9 | 6,8 |
| | | 6N138 | | 1 | 10 | μs | $I_F$ = 1.6mA, $R_L$ = 2.2kΩ | | |
| Propagation Delay Time To Logic High at Output | $t_{PLH}$* | 6N139 | | 5<br>1 | 60<br>7 | μs | $I_F$ = 0.5mA, $R_L$ = 4.7kΩ<br>$I_F$ = 12mA, $R_L$ = 270Ω | 9 | 6,8 |
| | | 6N138 | | 4 | 35 | μs | $I_F$ = 1.6mA, $R_L$ = 2.2kΩ | | |
| Common Mode Transient Immunity at Logic High Level Output | $CM_H$ | | | 500 | | V/μs | $I_F$ = 0mA, $R_L$ = 2.2kΩ, $R_{CC}$ = 0<br>$\|V_{cm}\|$ = 10$V_{p-p}$ | 10 | 9,10 |
| Common Mode Transient Immunity at Logic Low Level Output | $CM_L$ | | | −500 | | V/μs | $I_F$ = 1.6mA, $R_L$ = 2.2kΩ, $R_{CC}$ = 0<br>$\|V_{cm}\|$ = 10$V_{p-p}$ | 10 | 9,10 |

NOTES:

1. Derate linearly above 50°C free-air temperature at a rate of 0.4mA/°C.
2. Derate linearly above 50°C free-air temperature at a rate of 0.7mW/°C.
3. Derate linearly above 25°C free-air temperature at a rate of 0.7mA/°C.
4. Derate linearly above 25°C free-air temperature at a rate of 2.0mW/°C.
5. DC CURRENT TRANSFER RATIO is defined as the ratio of output collector current, $I_O$, to the forward LED input current, $I_F$, times 100%.
6. Pin 7 Open.
7. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
8. Use of a resistor between pin 5 and 7 will decrease gain and delay time. See Application Note 951-1 for more details.
9. Common mode transient immunity in Logic High level is the maximum tolerable (positive) $dV_{cm}/dt$ on the leading edge of the common mode pulse, $V_{cm}$, to assure that the output will remain in a Logic High state (i.e., $V_O > 2.0V$). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) $dV_{cm}/dt$ on the trailing edge of the common mode pulse signal, $V_{cm}$, to assure that the output will remain in a Logic Low state (i.e., $V_O < 0.8V$).
10. In applications where dV/dt may exceed 50,000V/μs (such as static discharge) a series resistor, $R_{CC}$, should be included to protect the detector IC from destructively high surge currents. The recommended value is $R_{CC} \approx \frac{1V}{0.15\ I_F\ (mA)}$ kΩ.
11. This is a proof test to validate the UL 220 Vac rating.

*JEDEC Registered Data.

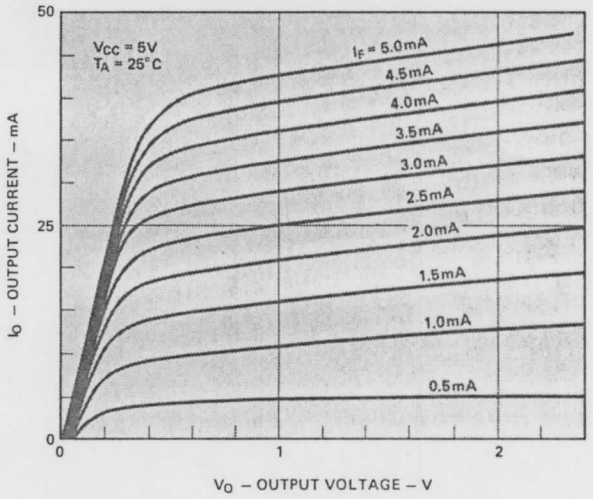



Figure 1. 6N139 DC Transfer Characteristics.

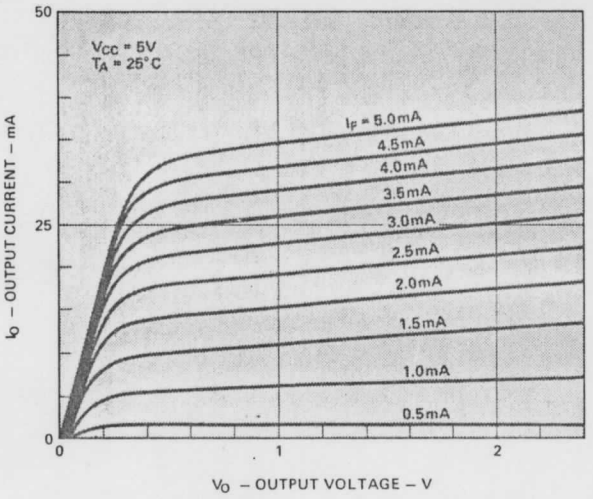



Figure 2. 6N138 DC Transfer Characteristics.

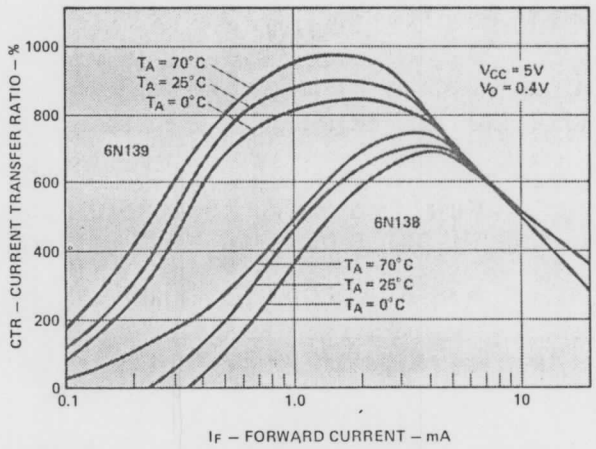



Figure 3. Current Transfer Ratio vs. Forward Current.

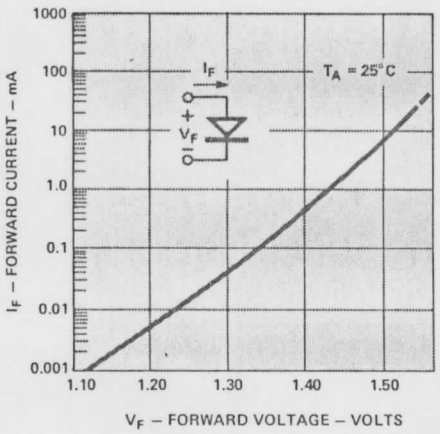



Figure 4. Input Diode Forward Current vs. Forward Voltage.

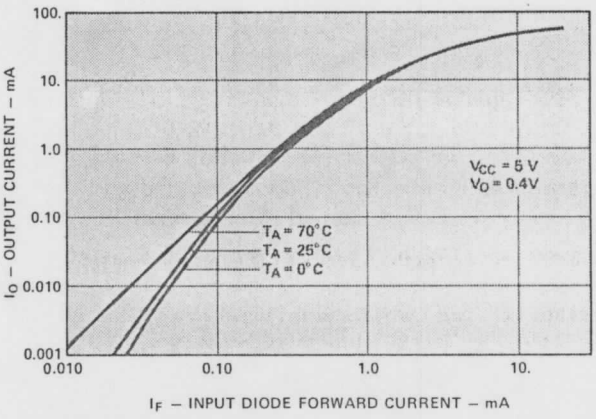



Figure 5. 6N139 Output Current vs. Input Diode Forward Current.

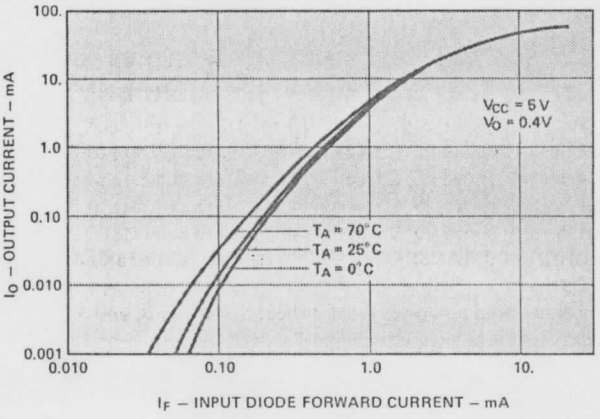



Figure 6. 6N138 Output Current vs. Input Diode Forward Current.

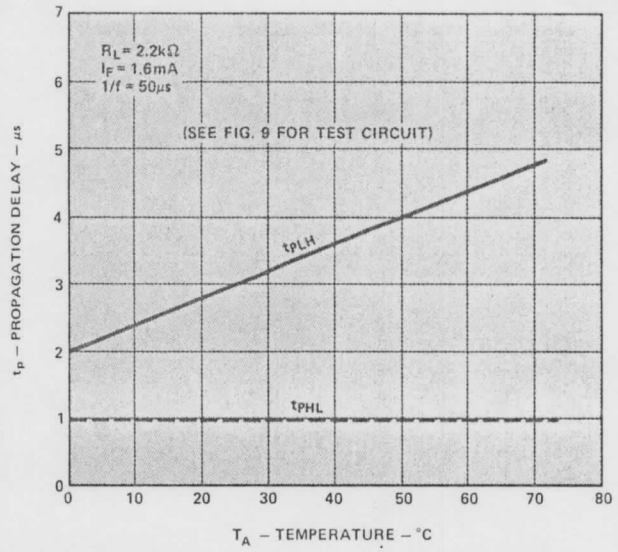



Figure 7. Propagation Delay vs. Temperature.

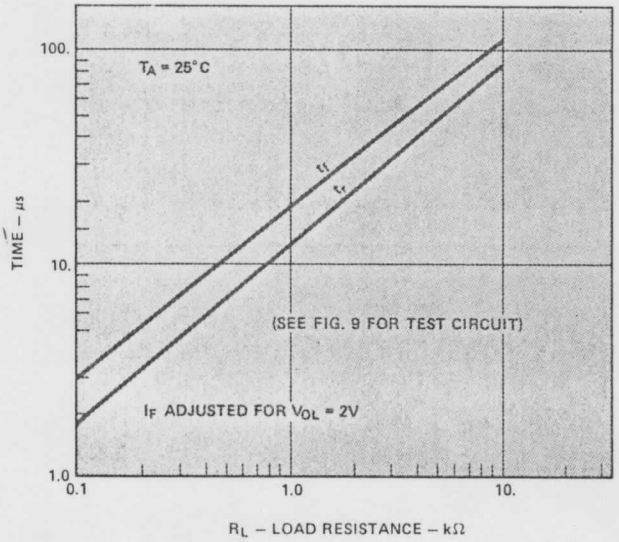



Figure 8. Non Saturated Rise and Fall Times vs. Load Resistance.

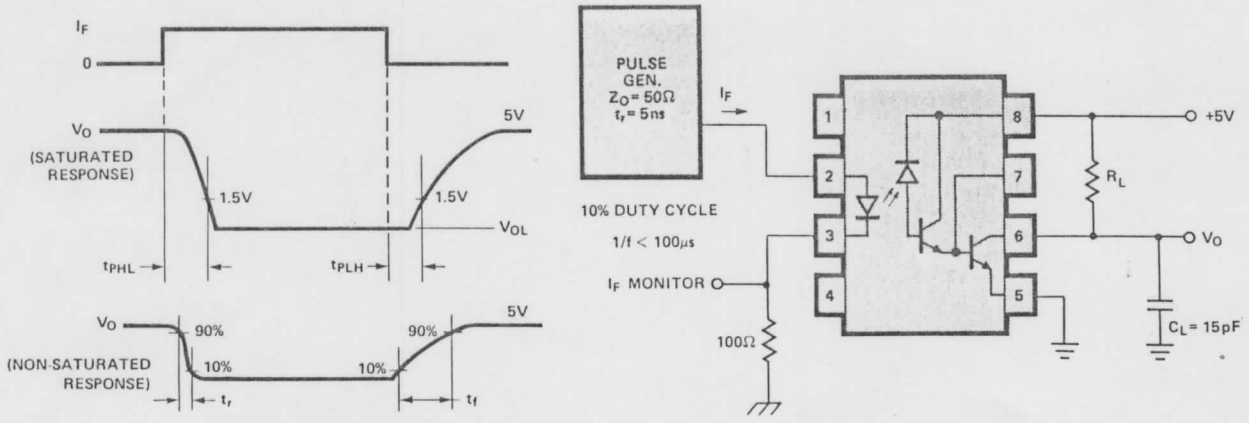



Figure 9. Switching Test Circuit.*

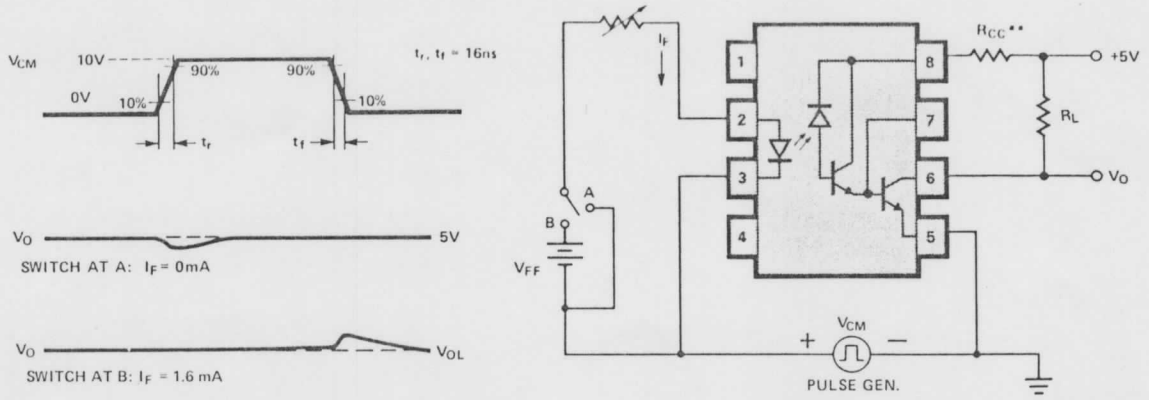



Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.

*JEDEC Registered Data.

**See Note 10

HEWLETT hp PACKARD

COMPONENTS

# DUAL TTL COMPATIBLE OPTOCOUPLER

HCPL-2630

TECHNICAL DATA APRIL 1979

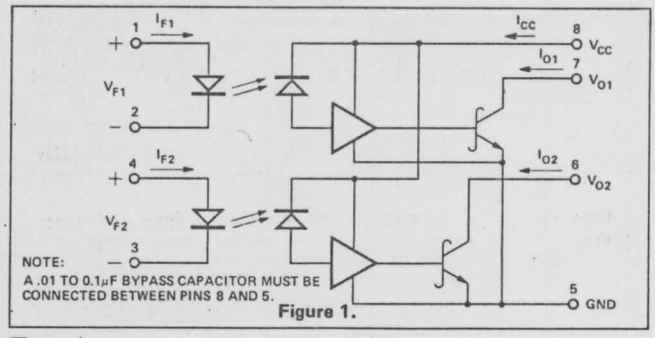



Figure 1.

## Features

- HIGH DENSITY PACKAGING
- DTL/TTL COMPATIBLE: 5V SUPPLY
- ULTRA HIGH SPEED
- LOW INPUT CURRENT REQUIRED
- HIGH COMMON MODE REJECTION
- GUARANTEED PERFORMANCE OVER TEMPERATURE
- RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361)
- 3000Vdc INSULATION VOLTAGE

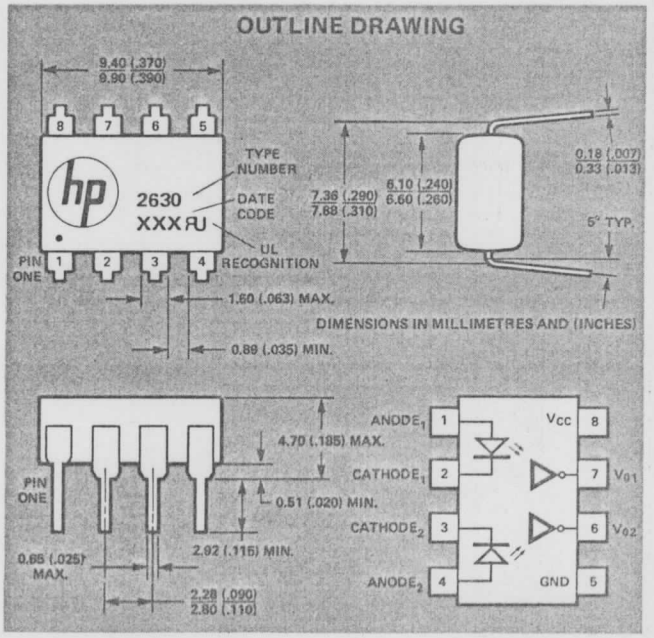
## Description/Applications

The HCPL-2630 consists of a pair of inverting optically coupled gates each with a GaAsP photon emitting diode and a unique integrated detector. The photons are collected in the detector by a photodiode and then amplified by a high gain linear amplifier that drives a Schottky clamped open collector output transistor. Each circuit is temperature, current and voltage compensated.

This unique dual coupler design provides maximum DC and AC circuit isolation between each input and output while achieving DTL/TTL circuit compatibility. The coupler operational parameters are guaranteed from 0°C to 70°C, such that a minimum input current of 5 mA in each channel will sink an eight gate fan-out (13 mA) at the output with 5 volt $V_{CC}$ applied to the detector. This isolation and coupling is achieved with a typical propagation delay of 50 nsec.

The HCPL-2630 can be used in high speed digital interface applications where common mode signals must be rejected such as for a line receiver and digital programming of floating power supplies, motors, and other machine control systems. The elimination of ground loops can be accomplished between system interfaces such as between a computer and a peripheral memory, printer, controller, etc.

The open collector output provides capability for bussing, strobing and "WIRED-OR" connection. In all applications, the dual channel configuration allows for high density packaging, increased convenience and more usable board space.




## Recommended Operating Conditions

| | Sym. | Min. | Max. | Units |
|---|---|---|---|---|
| Input Current, Low Level Each Channel | $I_{FL}$ | 0 | 250 | μA |
| Input Current, High Level Each Channel | $I_{FH}$ | 6.3* | 15 | mA |
| Supply Voltage, Output | $V_{CC}$ | 4.5 | 5.5 | V |
| Fan Out (TTL Load) Each Channel | N | | 8 | |
| Operating Temperature | $T_A$ | 0 | 70 | °C |

## Absolute Maximum Ratings

(No derating required up to 70°C)

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... 0°C to +70°C
Lead Solder Temperature ..... 260°C for 10s
(1.6mm below seating plane)
Peak Forward Input
Current (each channel) ..... 30mA (≤1 msec Duration)
Average Forward Input Current (each channel) ..... 15mA
Reverse Input Voltage (each channel) ..... 5V
Supply Voltage – $V_{CC}$ ..... 7V (1 Minute Maximum)
Output Current – $I_O$ (each channel) ..... 16 mA
Output Voltage – $V_O$ (each channel) ..... 7V
Output Collector Power Dissipation ..... 60 mW

*6.3mA condition permits at least 20% CTR degradation guardband. Initial switching threshold is 5mA or less.

# Electrical Characteristics

## OVER RECOMMENDED TEMPERATURE ($T_A$ = 0°C TO 70°C) UNLESS OTHERWISE NOTED

| Parameter | Symbol | Min. | Typ.* | Max. | Units | Test Conditions | Figure | Note |
|---|---|---|---|---|---|---|---|---|
| High Level Output Current | $I_{OH}$ | | 50 | 250 | μA | $V_{CC}$ = 5.5V, $V_O$ = 5.5V, $I_F$ = 250μA | | 3 |
| Low Level Output Voltage | $V_{OL}$ | | 0.5 | 0.6 | V | $V_{CC}$ = 5.5V, $I_F$ = 5mA $I_{OL}$ (Sinking) = 13mA | 3 | 3 |
| High Level Supply Current | $I_{CCH}$ | | 14 | 30 | mA | $V_{CC}$ = 5.5V, $I_F$ = 0 (Both Channels) | | |
| Low Level Supply | $I_{CCL}$ | | 26 | 36 | mA | $V_{CC}$ = 5.5V, $I_F$ = 10mA (Both Channels) | | |
| Input – Output Insulation Leakage Current | $I_{I-O}$ | | | 1.0 | μA | Relative Humidity = 45% $T_A$ = 25°C, t = 5s, $V_{I-O}$ = 3000Vdc | | 4 |
| Resistance (Input-Output) | $R_{I-O}$ | | $10^{12}$ | | Ω | $V_{I-O}$ = 500V, $T_A$ = 25°C | | 4 |
| Capacitance (Input-Output) | $C_{I-O}$ | | 0.6 | | pF | f = 1MHz, $T_A$ = 25°C | | 4 |
| Input Forward Voltage | $V_F$ | | 1.5 | 1.75 | V | $I_F$ = 10mA, $T_A$ = 25°C | 4 | 7,3 |
| Input Reverse Breakdown Voltage | $BV_R$ | 5 | | | V | $I_R$ = 10μA, $T_A$ = 25°C | | |
| Input Capacitance | $C_{IN}$ | | 60 | | pF | $V_F$ = 0, f = 1MHz | | 3 |
| Input-Input Insulation Leakage Current | $I_{I-I}$ | | 0.005 | | μA | Relative Humidity = 45%, t=5s, $V_{I-I}$=500V | | 8 |
| Resistance (Input-Input) | $R_{I-I}$ | | $10^{11}$ | | Ω | $V_{I-I}$ = 500V | | 8 |
| Capacitance (Input-Input) | $C_{I-I}$ | | 0.25 | | pF | f = 1MHz | | 8 |
| Current Transfer Ratio | CTR | | 700 | | % | $I_F$ = 5.0mA, $R_L$ = 100Ω | 2 | 6 |

*All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C

# Switching Characteristics at $T_A$=25°C, $V_{CC}$=5V

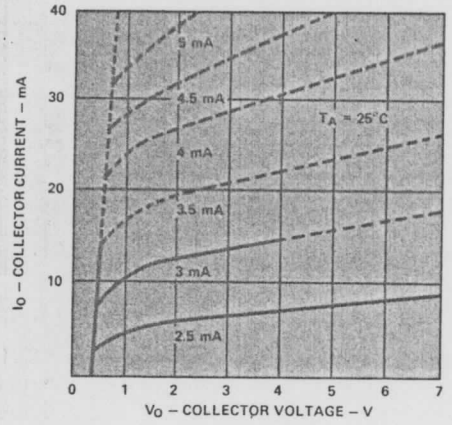
## EACH CHANNEL

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions | Figure | Note |
|---|---|---|---|---|---|---|---|---|
| Propagation Delay Time to High Output Level | $t_{PLH}$ | | 55 | 75 | ns | $R_L$ = 350 Ω, $C_L$ = 15pF, $I_F$ = 7.5mA | 6,7 | 1 |
| Propagation Delay Time to Low Output Level | $t_{PHL}$ | | 40 | 75 | ns | $R_L$ = 350 Ω, $C_L$ = 15pF, $I_F$ = 7.5mA | 6,7 | 2 |
| Output Rise-Fall Time (10-90%) | $t_r$, $t_f$ | | 25 | | ns | $R_L$ = 350 Ω, $C_L$ = 15pF, $I_F$ = 7.5mA | | |
| Common Mode Transient Immunity at High Output Level | $CM_H$ | | 50 | | V/μs | $V_{CM}$ = 10$V_{p-p}$, $R_L$ = 350 Ω, $V_O$ (min.) = 2V, $I_F$ = 0mA | 9 | 5 |
| Common Mode Transient Immunity at Low Output Level | $CM_L$ | | -150 | | V/μs | $V_{CM}$ = 10$V_{p-p}$, $R_L$ = 350 Ω, $V_O$ (max.) = 0.8V $I_F$ = 7.5mA | 9 | 5 |

**NOTE:** It is essential that a bypass capacitor (.01μF to 0.1μF, ceramic) be connected from pin 8 to pin 5. Total lead length between both ends of the capacitor and the isolator pins should not exceed 20mm. Failure to provide the bypass may impair the switching properties (Figure 5).

NOTES:

1. The $t_{PLH}$ propagation delay is measured from the 3.75 mA point on the trailing edge of the input pulse to the 1.5V point on the trailing edge of the output pulse.
2. The $t_{PHL}$ propagation delay is measured from the 3.75 mA point on the leading edge of the input pulse to the 1.5V point on the leading edge of the output pulse.
3. Each channel.
4. Measured between pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
5. Common mode transient immunity in Logic High level is the maximum tolerable (positive) $dV_{CM}/dt$ on the leading edge of the common mode pulse, $V_{CM}$, to assure that the output will remain in a Logic High state (i.e., $V_O > 2.0V$). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) $dV_{CM}/dt$ on the trailing edge of the common mode pulse signal, $V_{CM}$, to assure that the output will remain in a Logic Low state (i.e., $V_O < 0.8V$).
6. DC Current Transfer Ratio is defined as the ratio of the output collector current to the forward bias input current times 100%.
7. At 10mA VF decreases with increasing temperature at the rate of 1.9mV/°C.
8. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.




NOTE: Dashed characteristics indicate pulsed operation.

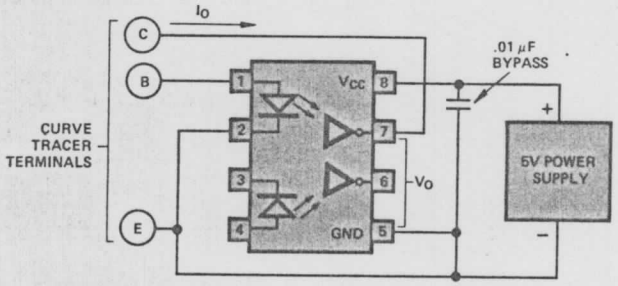
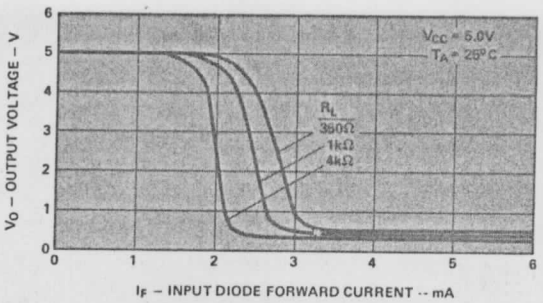



Figure 2. Optocoupler Transfer Characteristics.



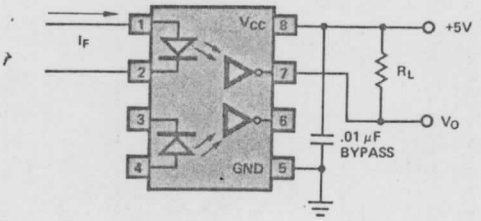




Figure 3. Input-Output Characteristics.

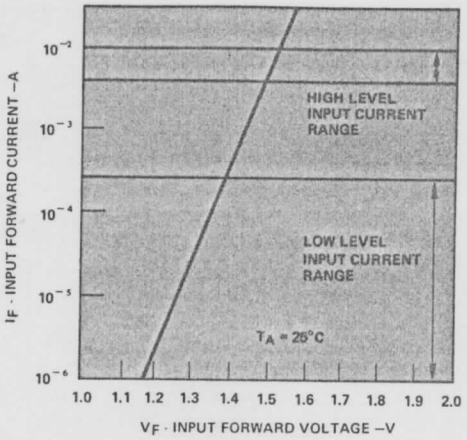



Figure 4. Input Diode Forward Characteristic

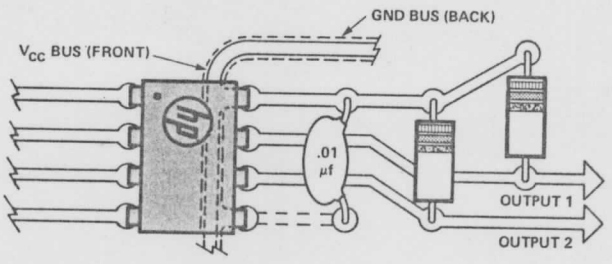



Figure 5. Recommended Printed Circuit Board Layout.

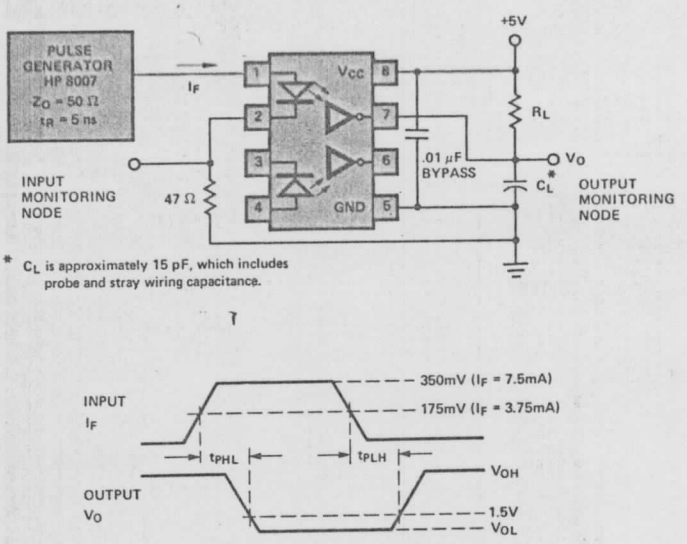






Figure 6. Test Circuit for $t_{PHL}$ and $t_{PLH}$.

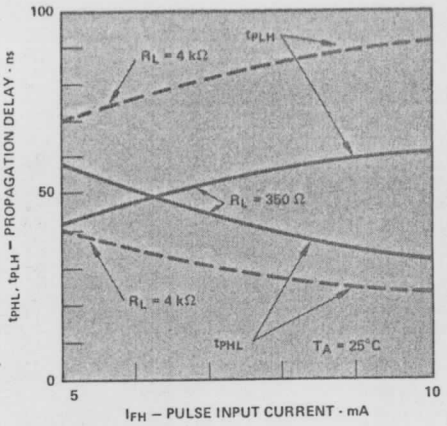



Figure 7. Propagation Delay, $t_{PHL}$ and $t_{PLH}$ vs. Pulse Input Current, $I_{FH}$.

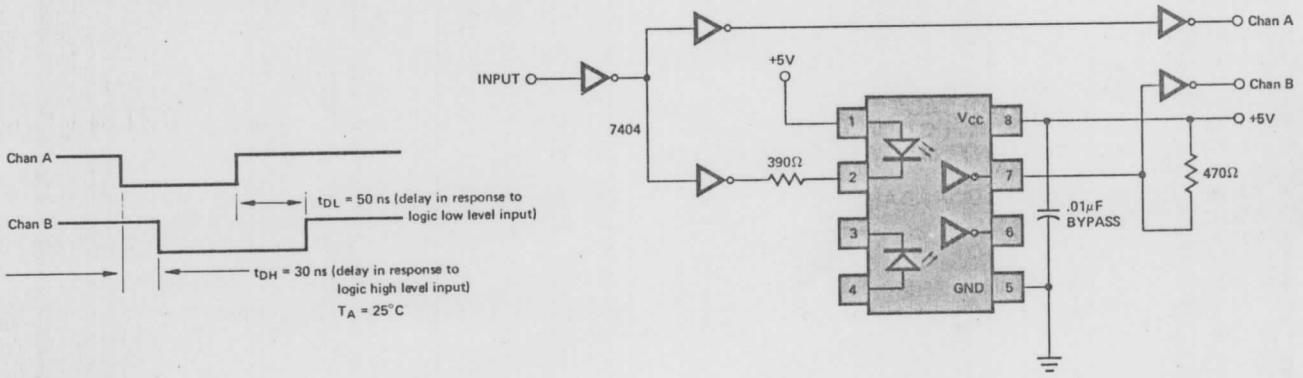



Figure 8. Response Delay Between TTL Gates.

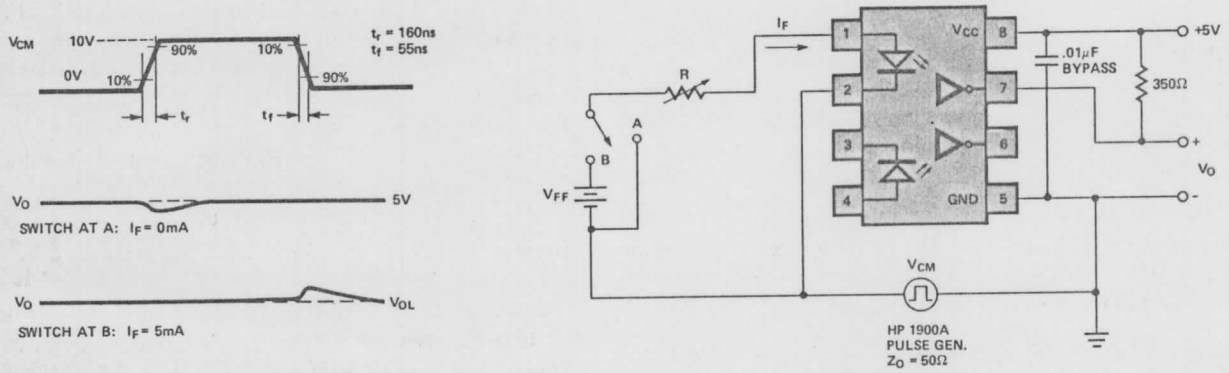



Figure 9. Test Circuit for Transient Immunity and Typical Waveforms.